

1/17

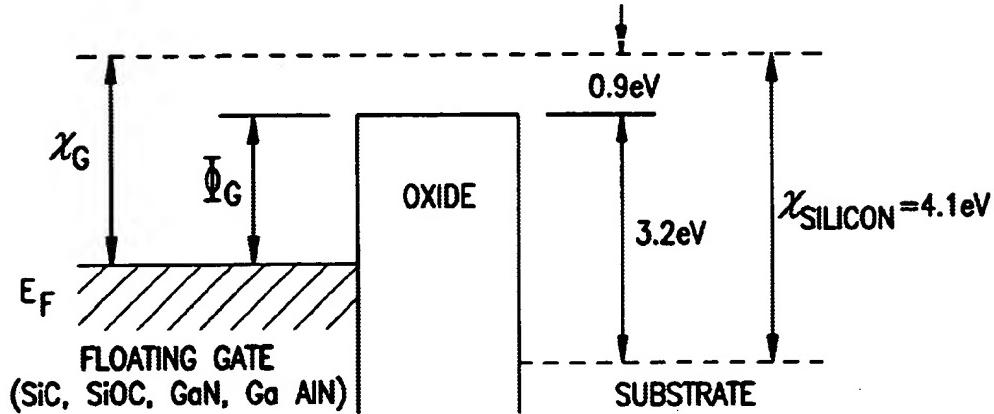


FIG. 1A
(PRIOR ART)

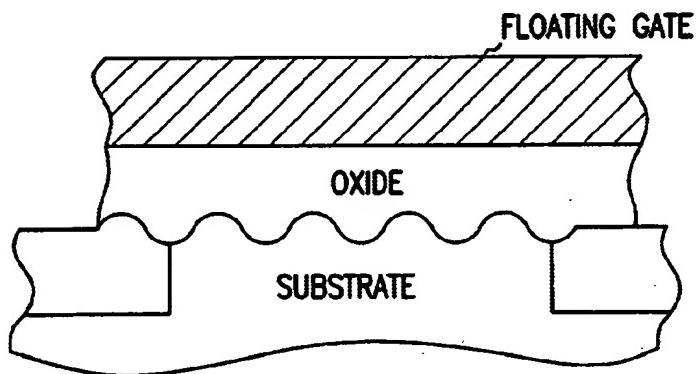


FIG. 1B
(PRIOR ART)

2/17

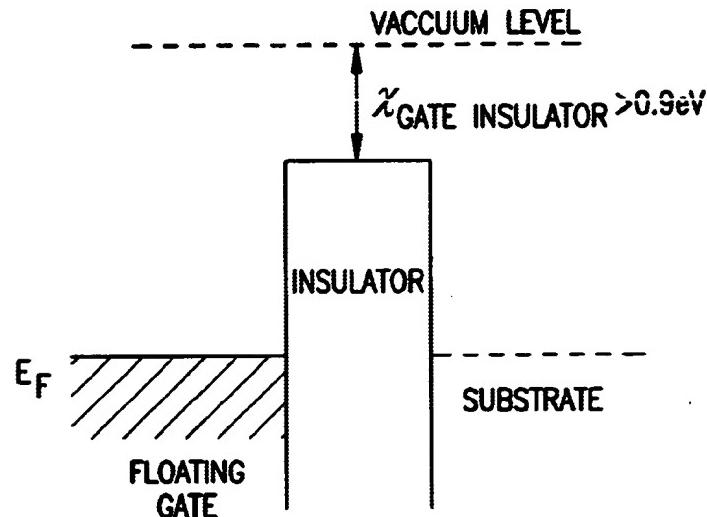


FIG. 1C
(PRIOR ART)

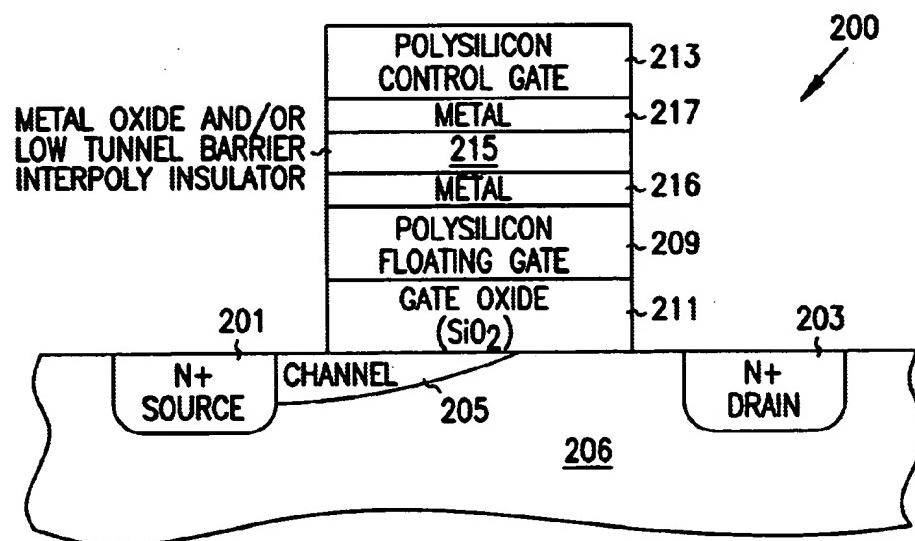


FIG. 2



3/17

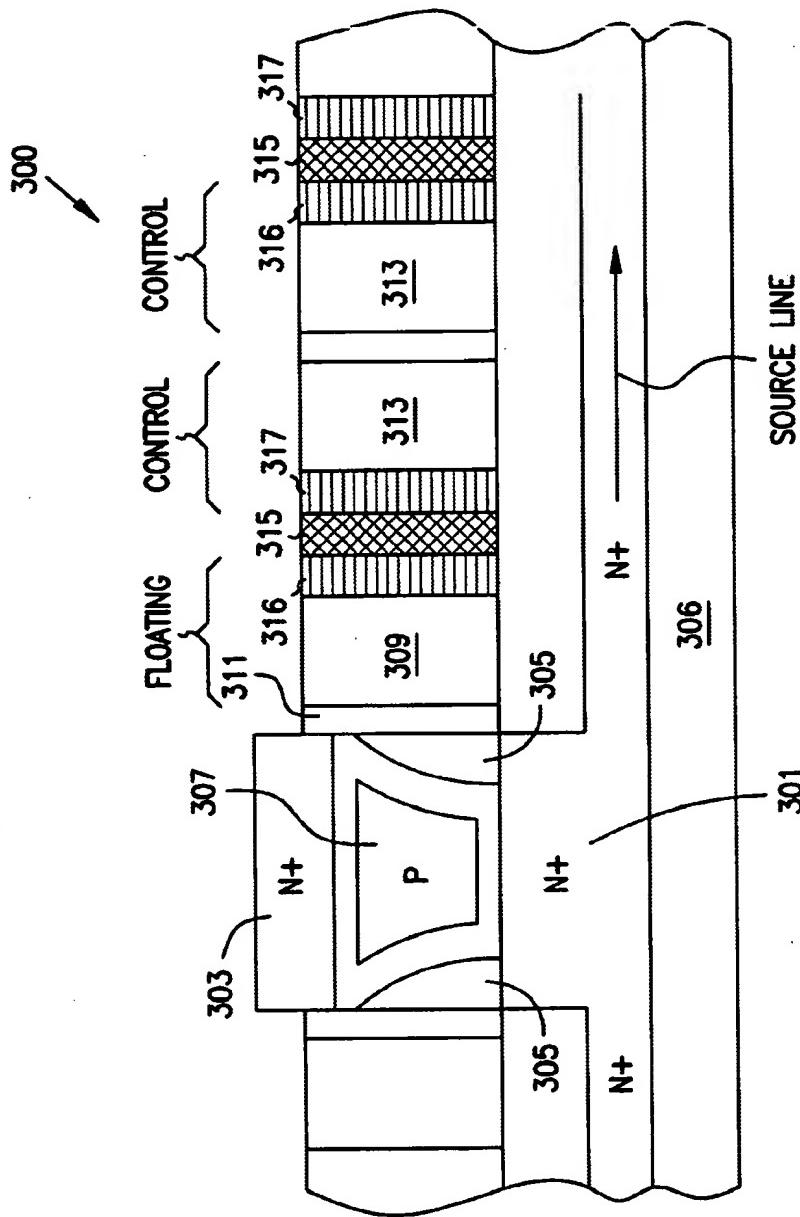
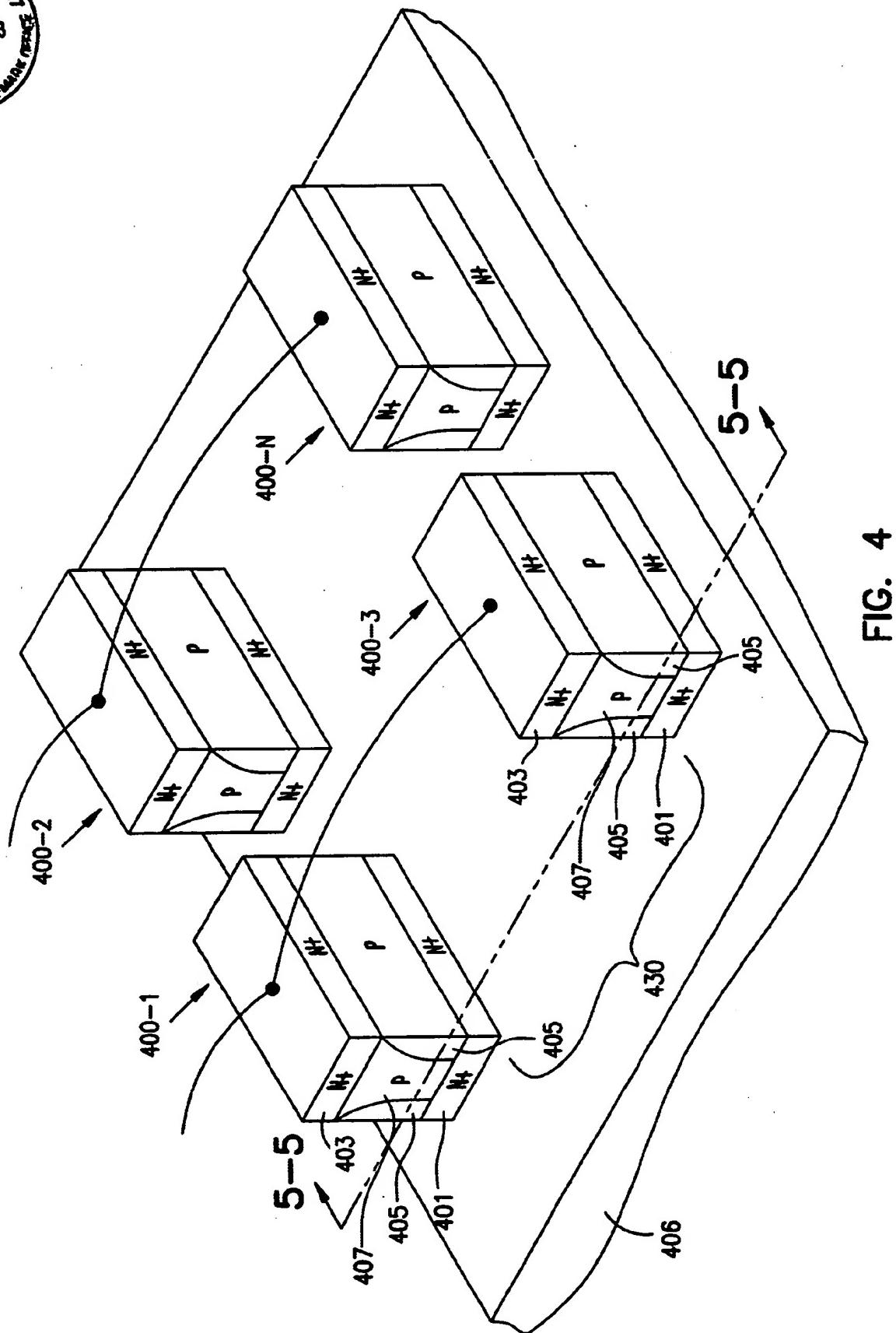


FIG. 3



4/17





5/17

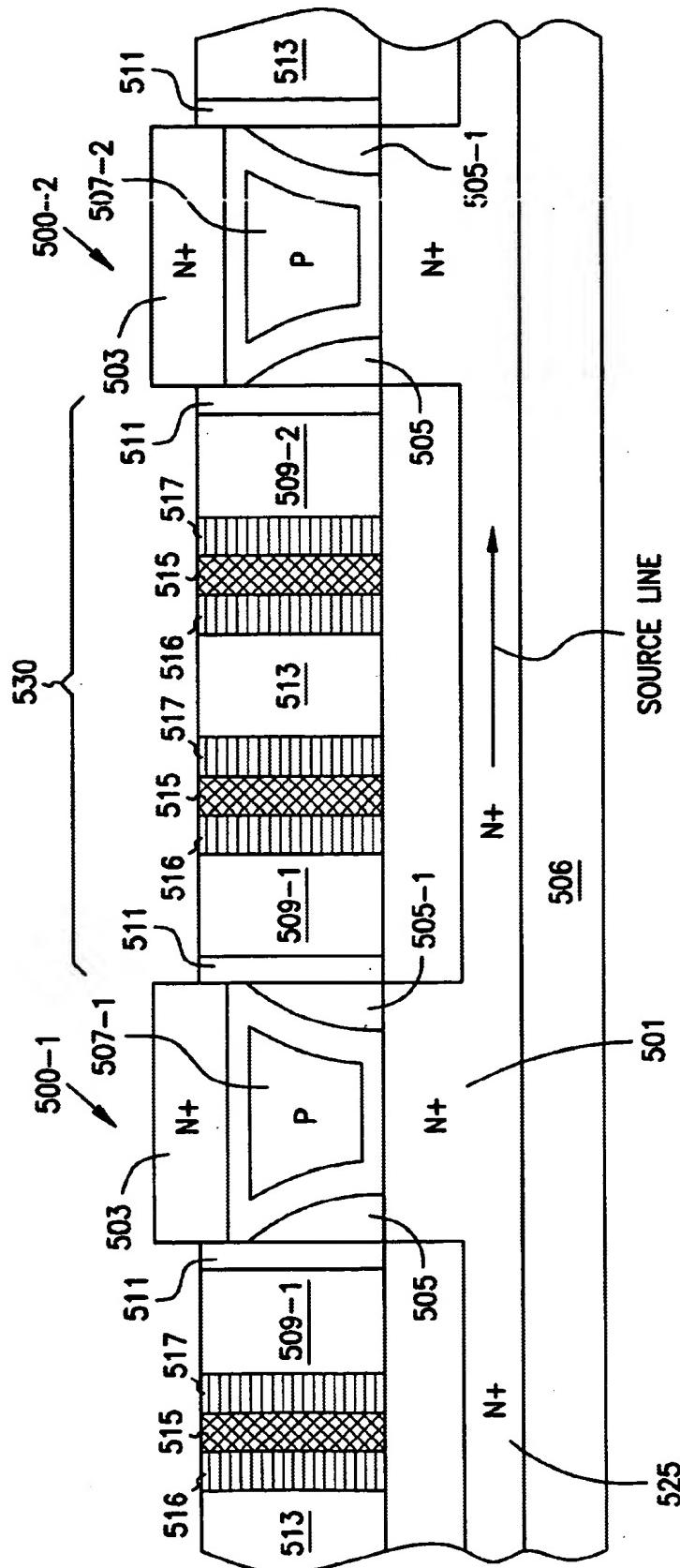


FIG. 5A



6/17

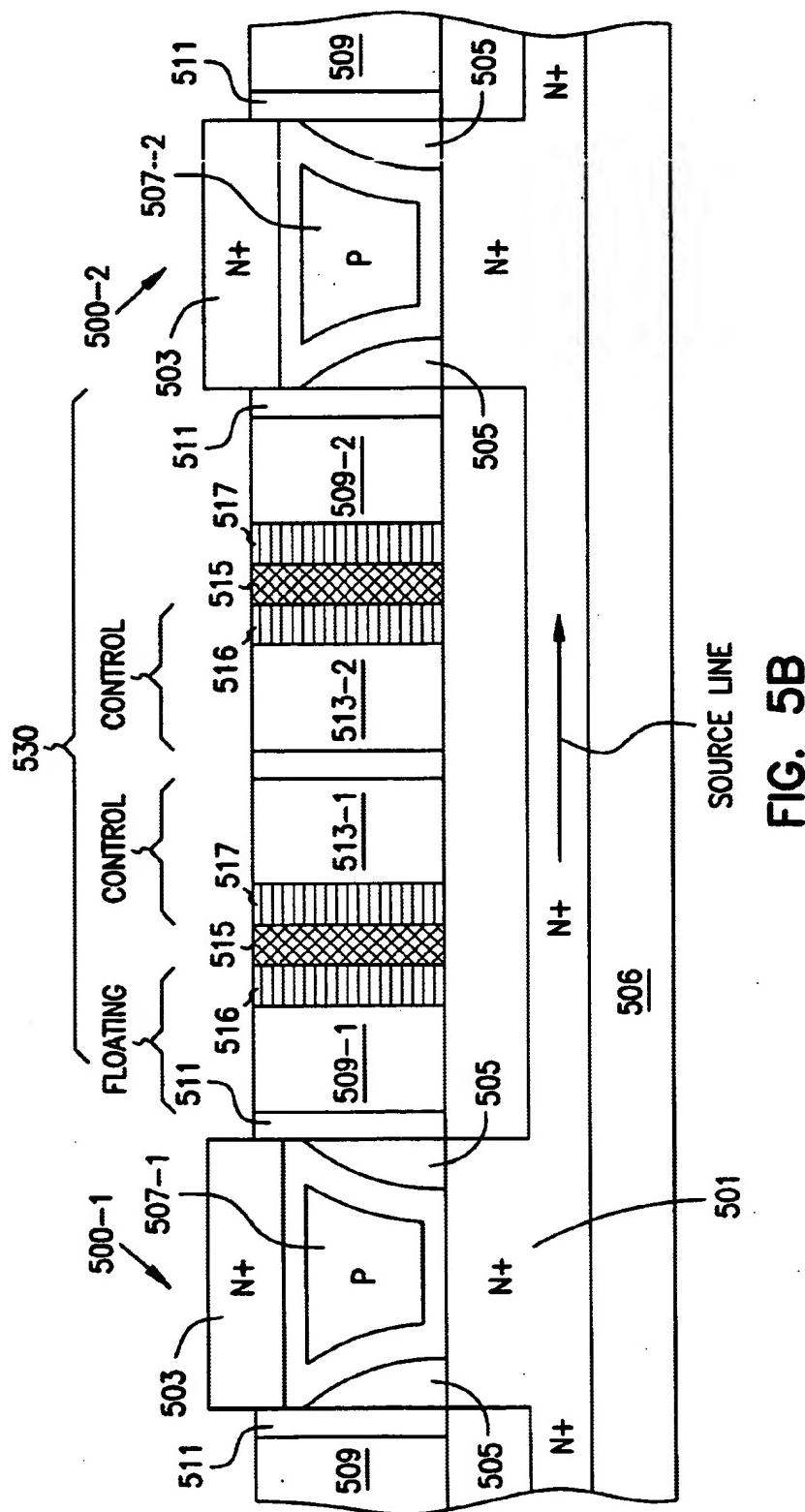


FIG. 5B



7/17

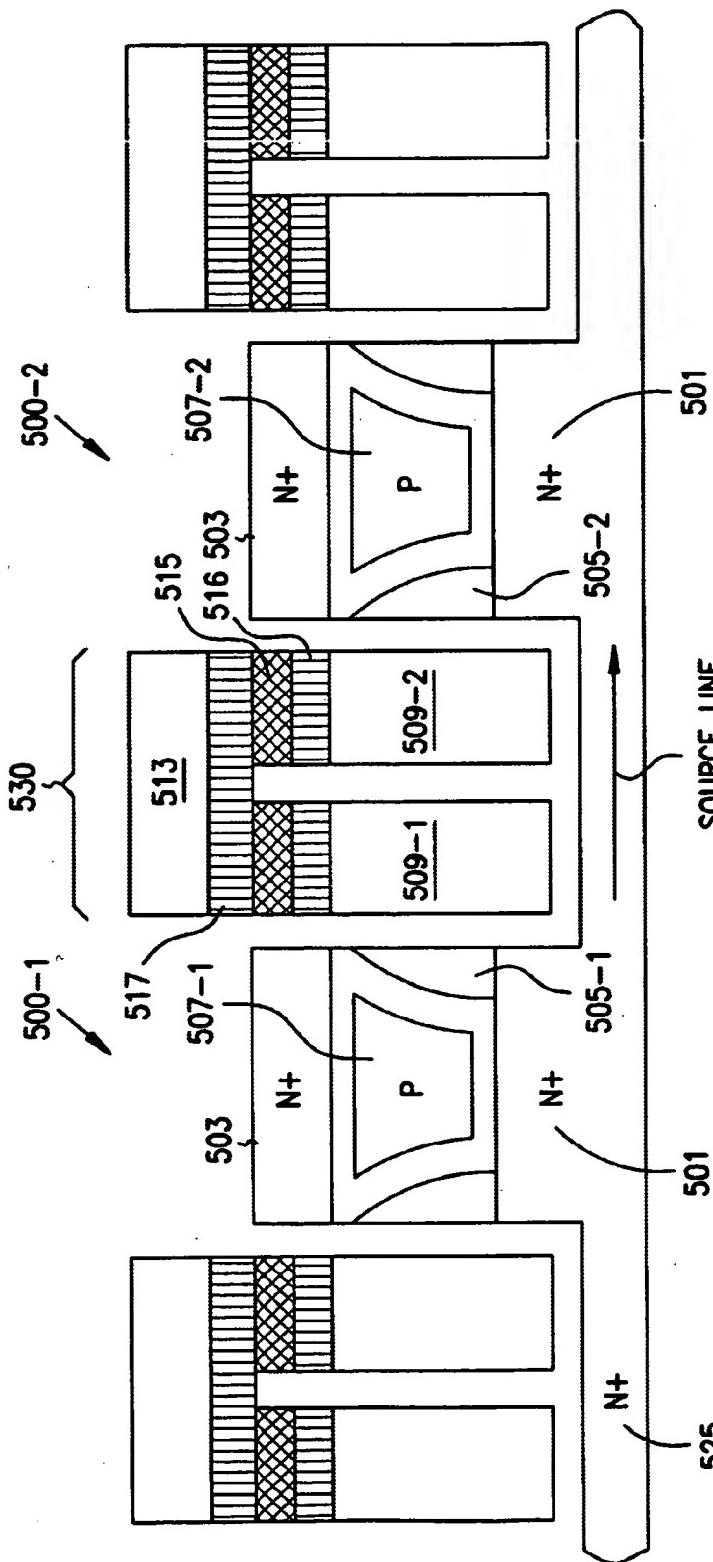


FIG. 5C



8/17

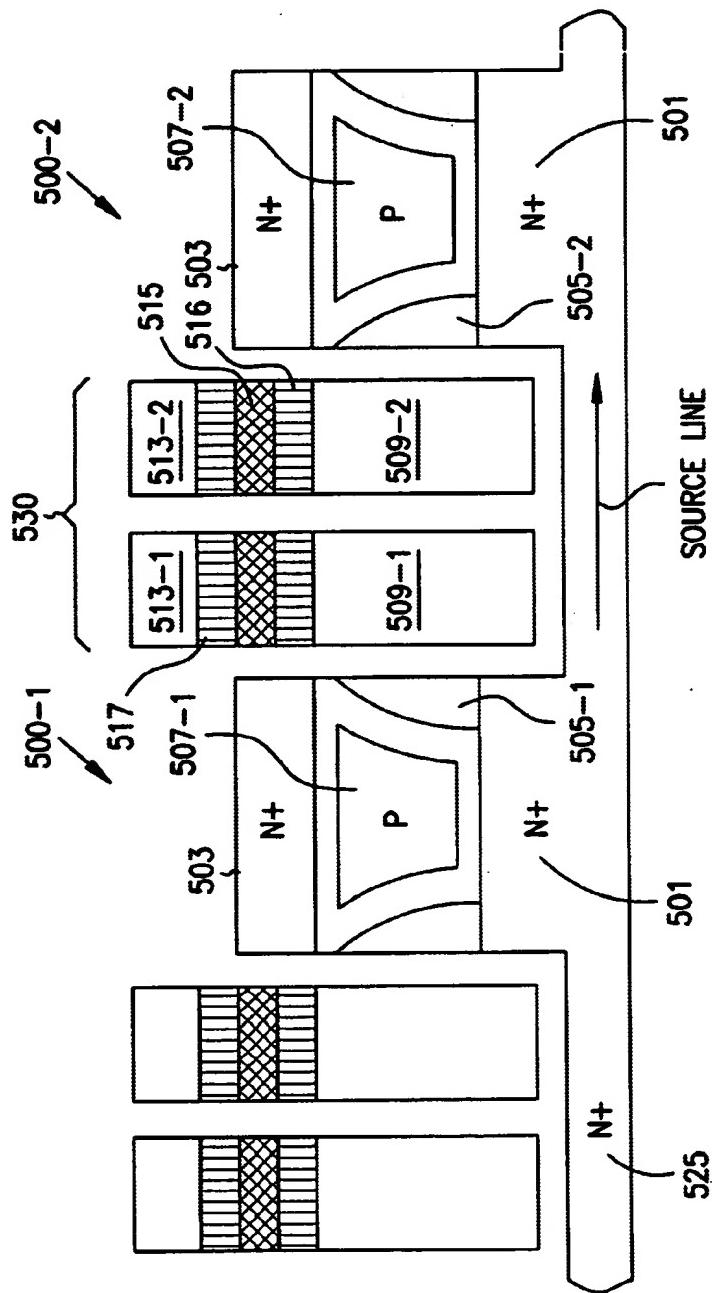


FIG. 5D



9/17

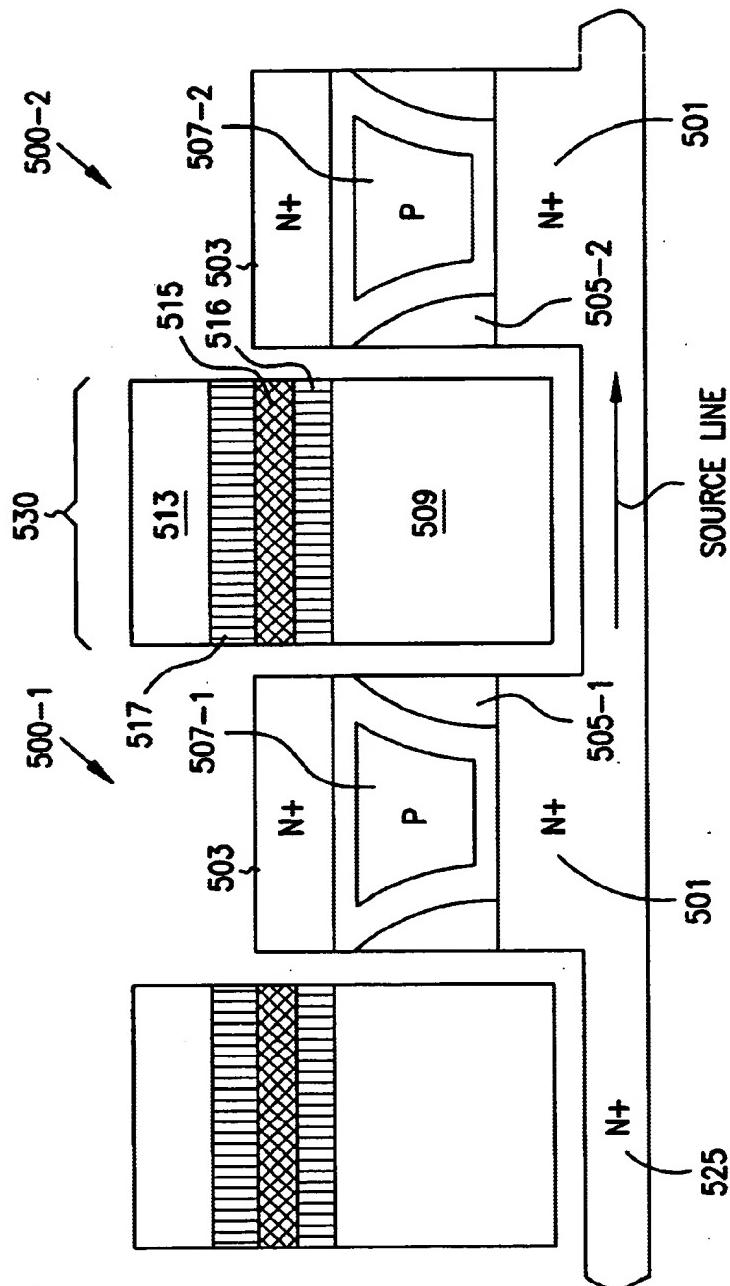


FIG. 5E



10/17

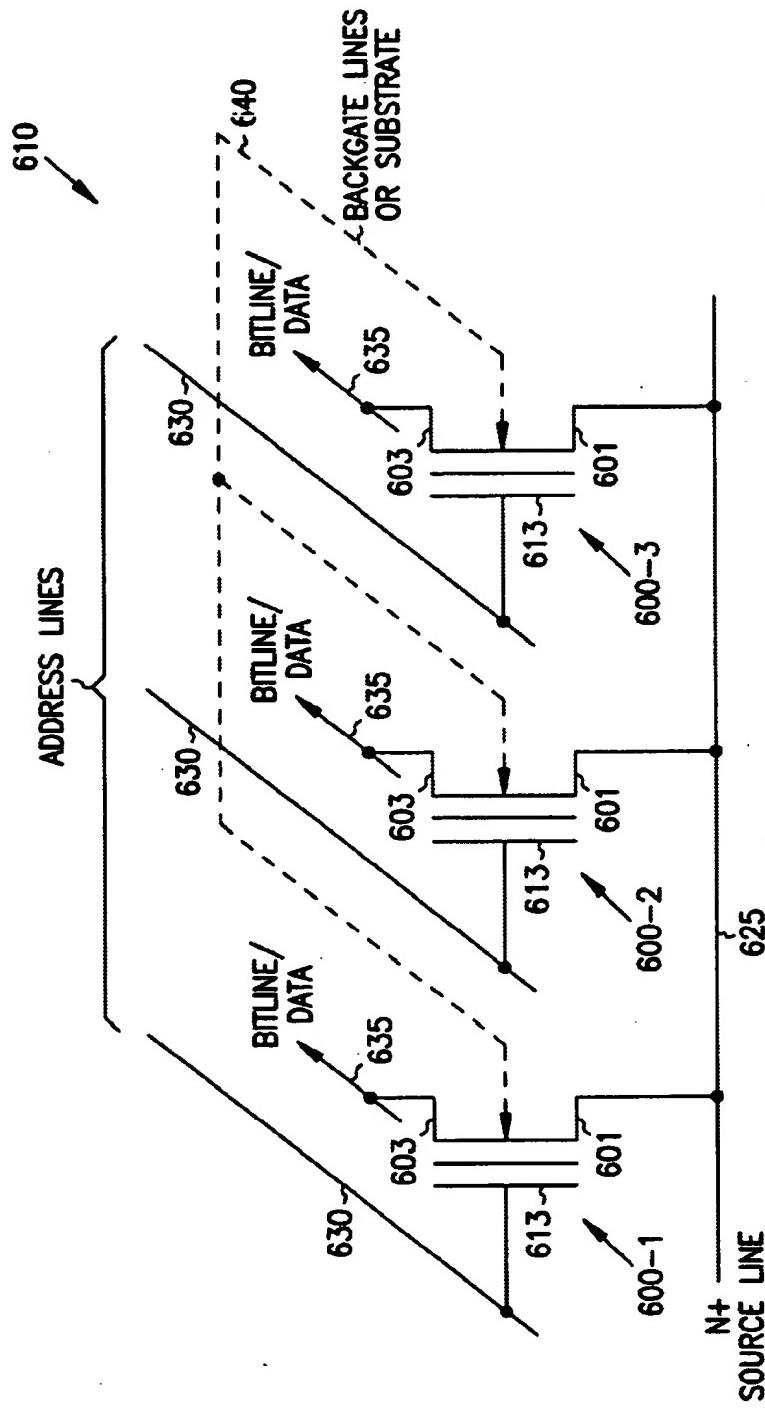


FIG. 6A



11/17

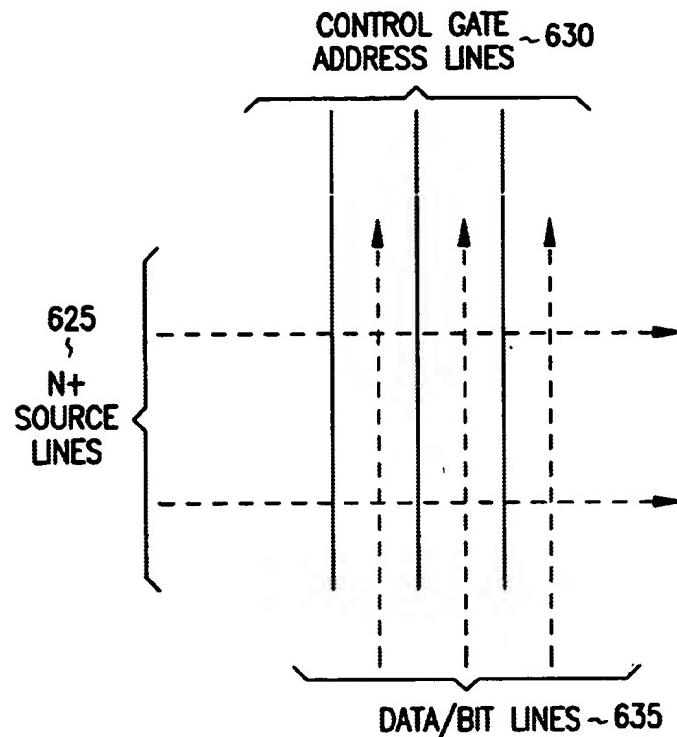


FIG. 6B

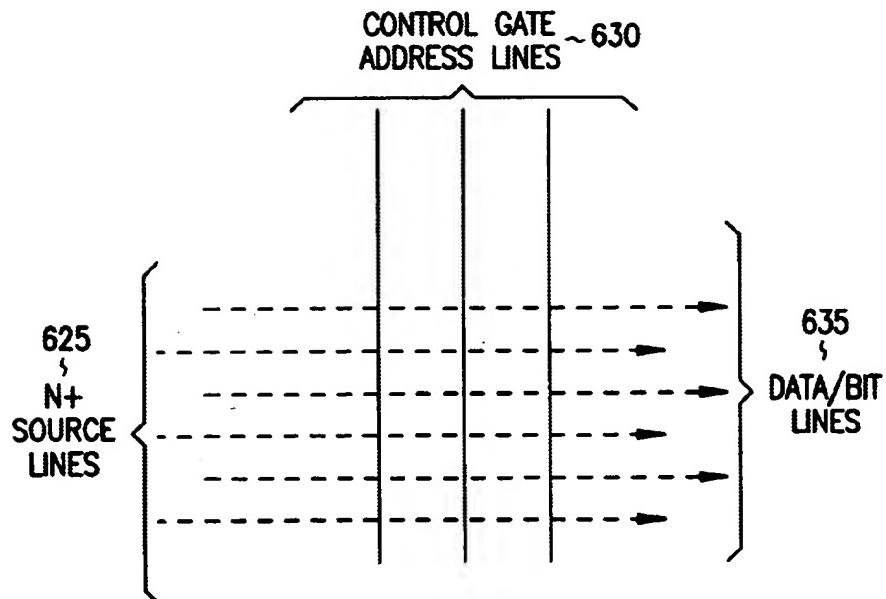


FIG. 6C



12/17

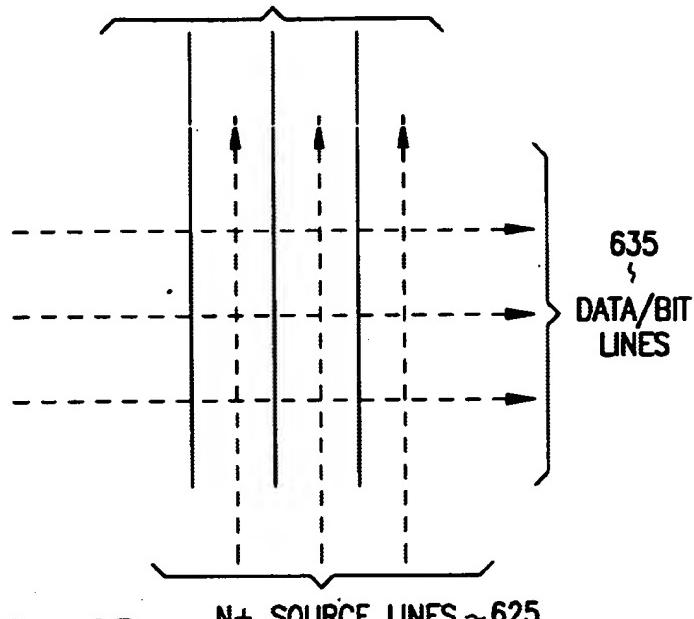
CONTROL GATE ~630
ADDRESS LINES

FIG. 6D

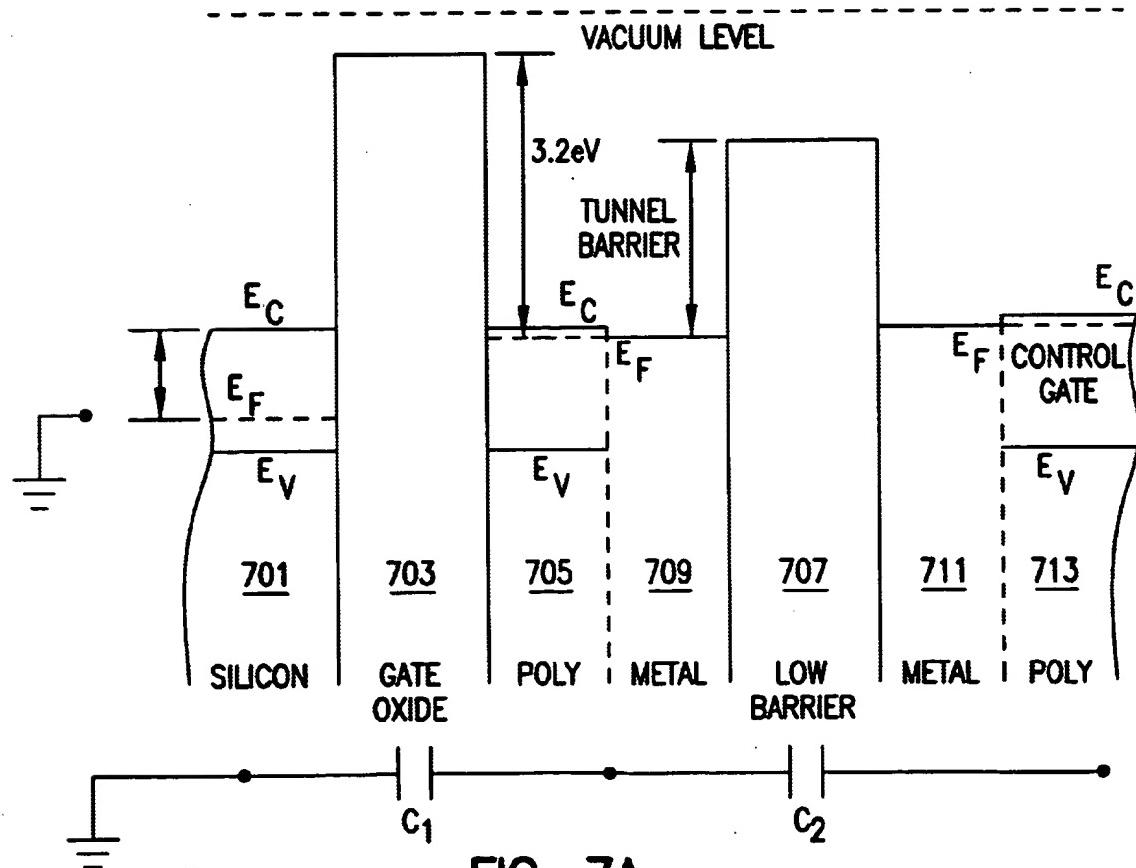


FIG. 7A



13/17

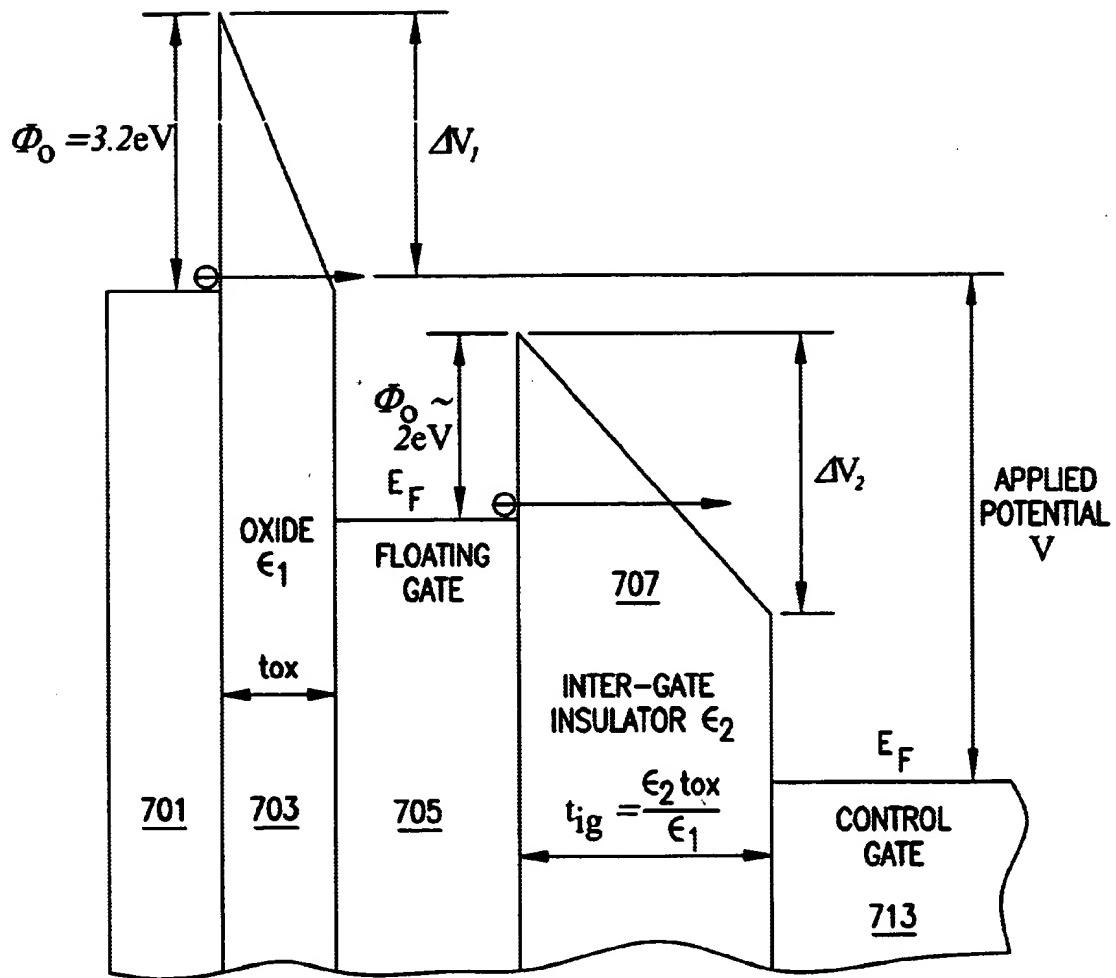
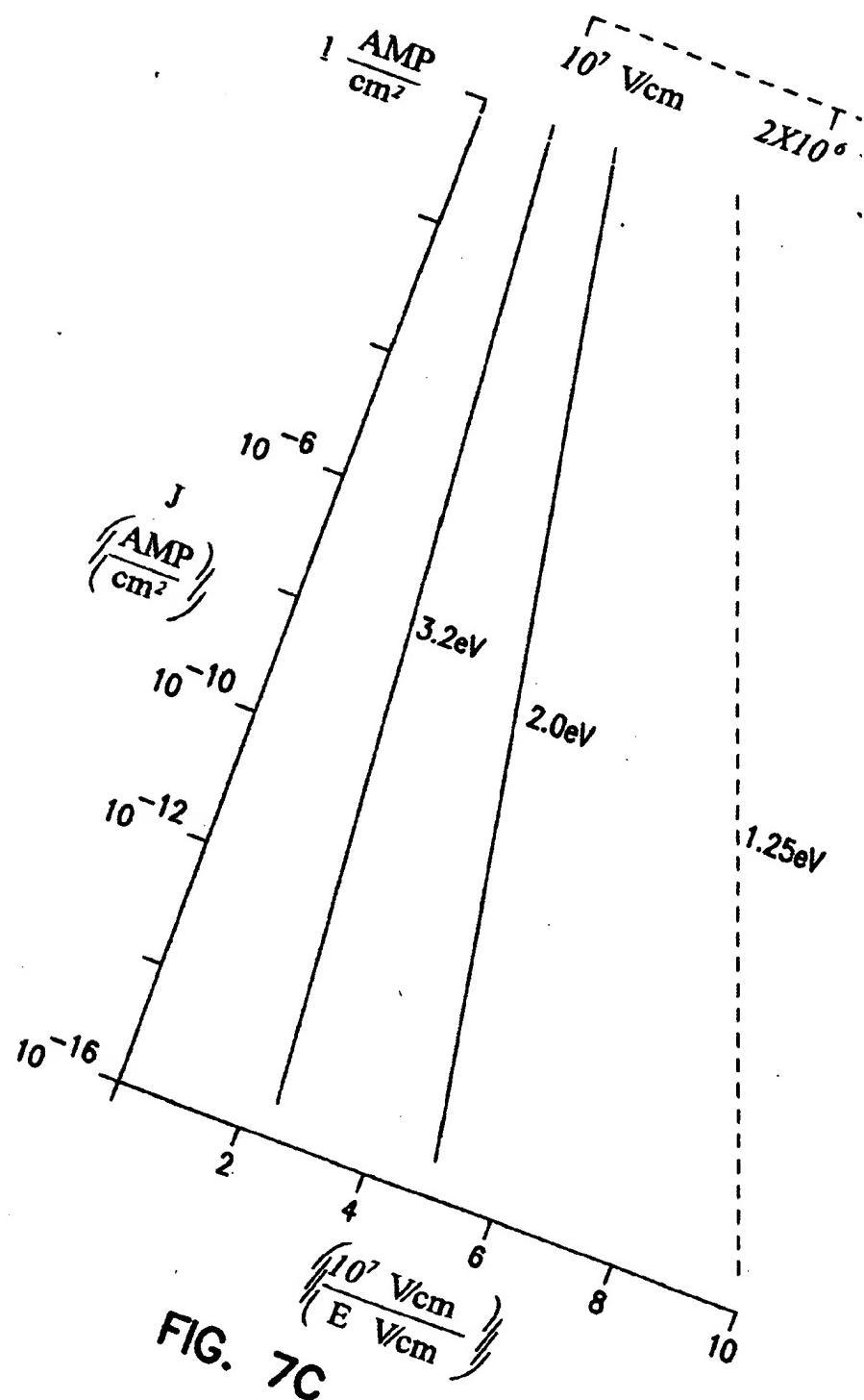


FIG. 7B

O I P E JCB7
SEP 22 2003
PATENT & TRADEMARK OFFICE

TITLE: IN-SERVICE PROGRAMMABLE LOGIC ARRAYS WITH L
INVENTOR'S NAME: L
DOCKET NO.: 1303.02;

14/17





15/17

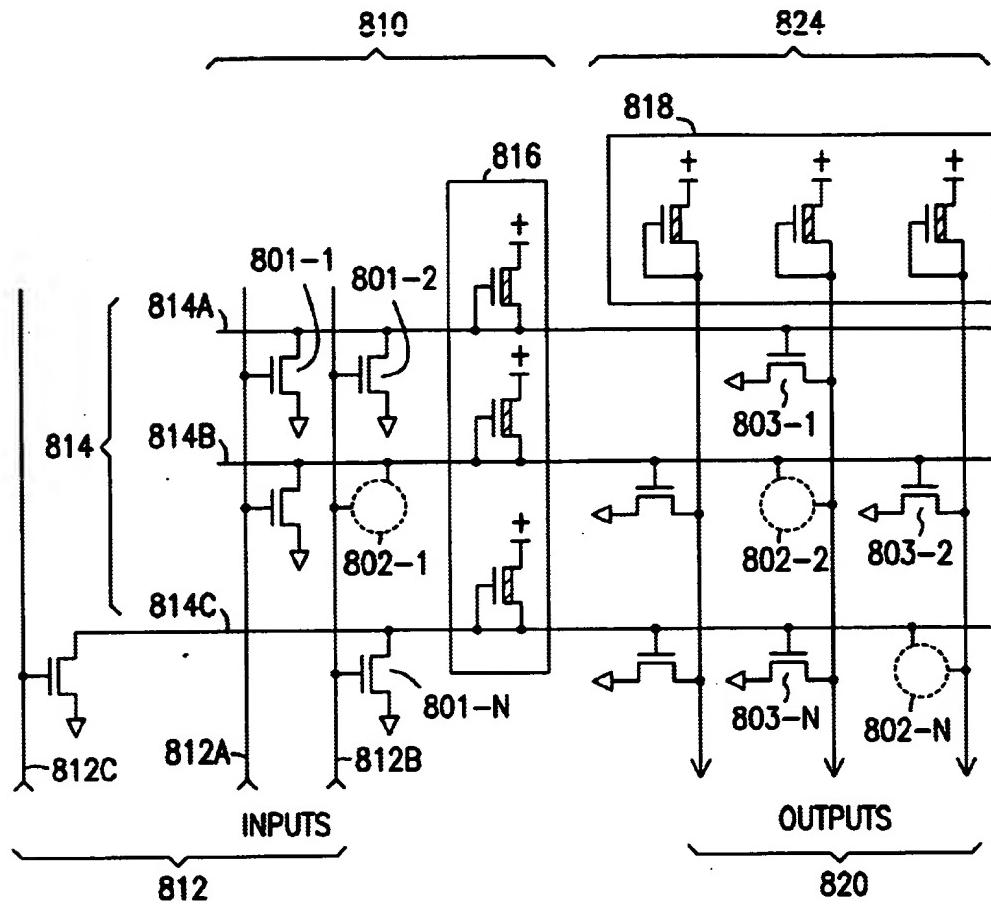


FIG. 8



16/17

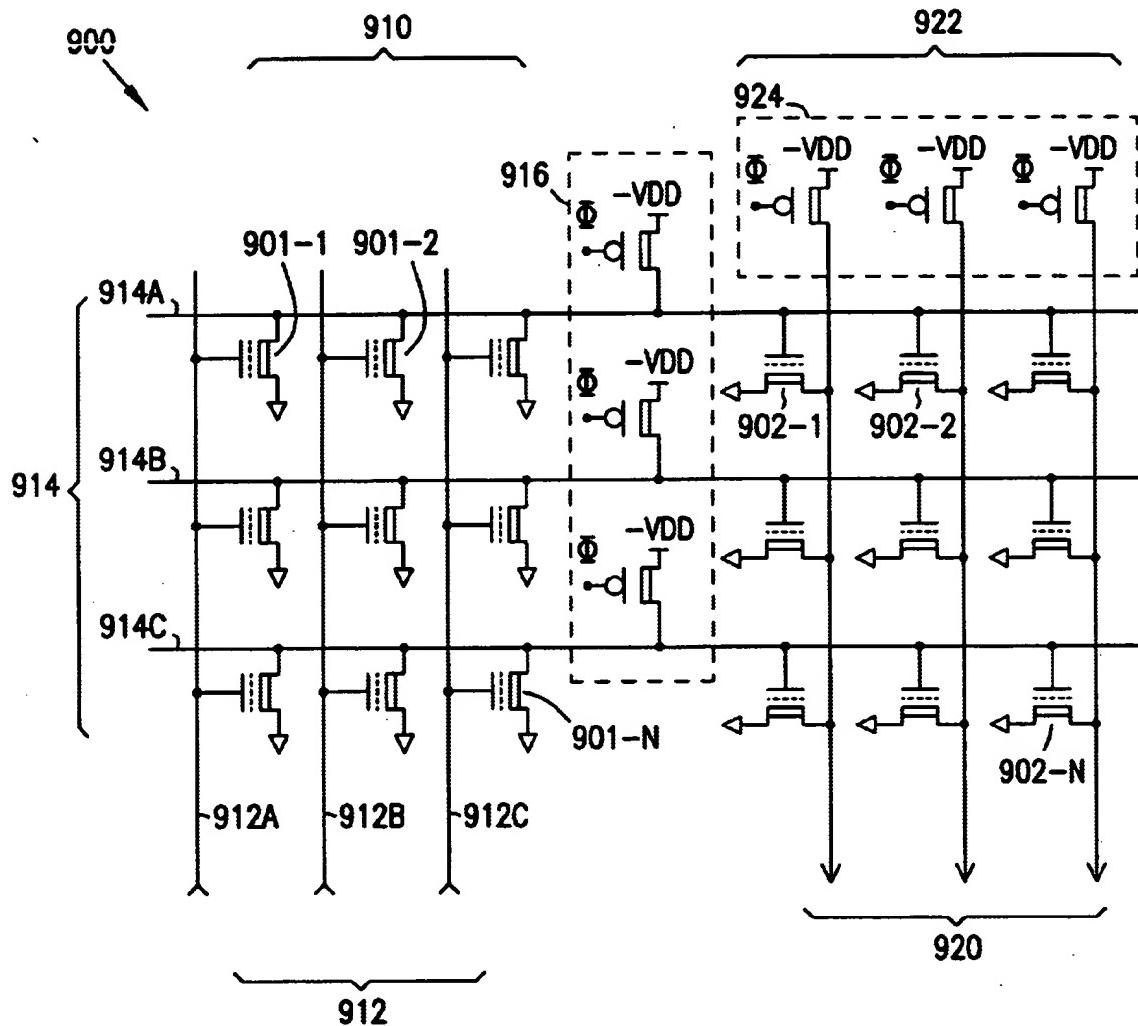


FIG. 9



TITLE: IN-SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
INVENTORS NAME: Leonard Forbes
DOCKET NO.: 1303.027US1

17/17

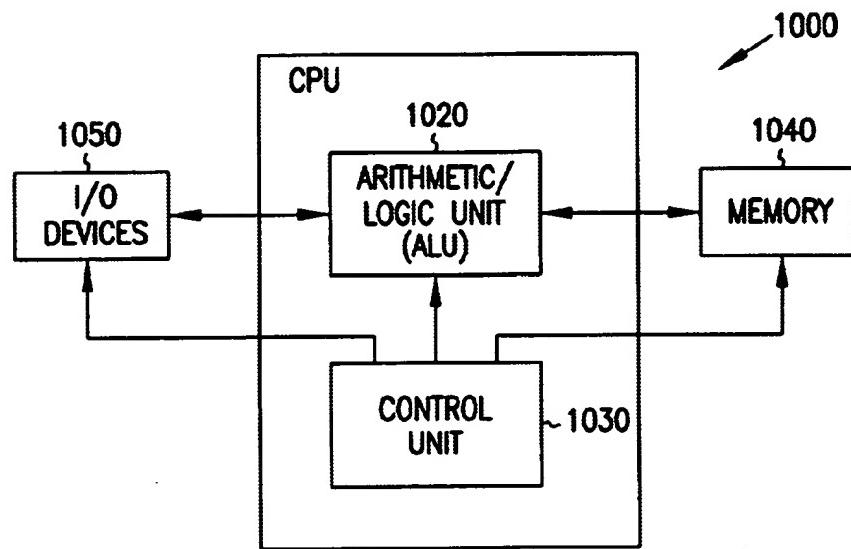


FIG. 10